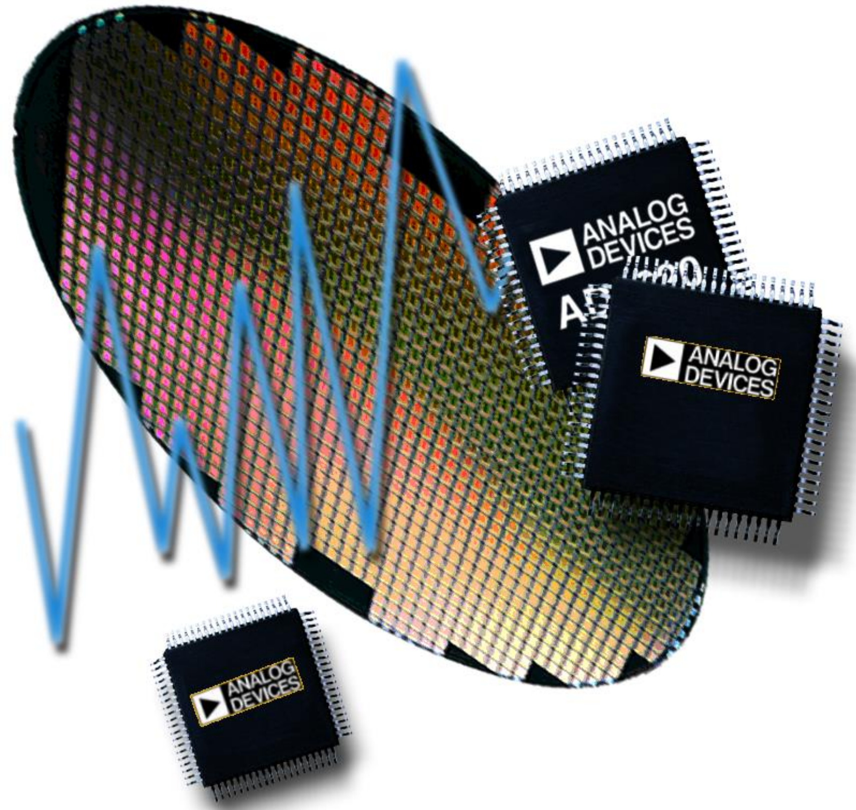

Reliability Report

Report Title: ADA4945-1 Die Revision Qualification

Report Number: 17557

Revision: A

Date: 28 October 2021

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the die revision on ADA4945-1 product in a 16-LFCSP package. The ADA4945-1 is a low noise, low distortion, fully differential amplifier with two selectable power modes. The device operates over a broad power supply range of 3 V to 10 V. The low dc offset, dc offset drift, and excellent dynamic performance of the ADA4945-1 makes it well suited for a variety of data acquisition and signal processing applications.

Table 1: ADA4945-1 Product Characteristics

Die/Fab

Die Id	TMKC67 E-T7
Die Size (mm)	1.13 x 1.03
Wafer Fabrication Site	E_TSMC0408
Wafer Fabrication Process	CBCMOS
Approximate Transistor Count	4,000
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu(0.5%)

Package/Assembly

Package	16-LFCSP
Body Size (mm)	3.00 x 3.00 x 0.00
Assembly Location	ASE (AEK)
Molding Compound	Sumitomo G700LYT
Die Attach Material	Hitachi EN 4900GC
Wire Type	MKE R 2N Gold
Wire Diameter (mil)	0.8
Lead Frame Material	Copper
Lead Finish	Matte Sn
Moisture Sensitivity Level	3
Maximum Peak Reflow Temperature (°C)	260

Description / Results of Tests Performed

Tables 2 through 3 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: LFCSP at ASE (AEK) Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
Temperature Cycling (TC) [1]	JESD22-A104	-65°C/+150°C, 500 Cycles	ADL6012	Q14865.10	77	0
				Q14865.8	77	0
				Q14865.9	77	0
Temperature Cycling (TC) [2]	JESD22-A104	-65°C/+150°C, 1,000 Cycles	AD74413R	Q14261.2	45	0
				Q14261.3	45	0
				Q14261.8	45	0
		-65°C/+150°C, 500 Cycles	ADG1411	Q14030.TC1	77	0
				Q14030.TC3	77	0
			ADL8001	Q14120.TC1	77	0
				Q14120.TC2	77	0
				Q14120.TC3	77	0
Temperature Humidity Bias (THB) [2]	JESD22-A101	85°C, 85%RH, Biased, 1,000 Hours	AD5941	Q14989.TH1A/B	77	0
				Q14989.TH2	77	0
				Q14989.TH3	77	0
			ADL8001	Q14120.TH5	77	0
				Q14120.TH5	77	0
			ADN8835	Q12788.TH1	45	0
				Q12788.TH2	45	0
				Q12788.TH3	45	0
			ADuCM4150	QL12865THB01	45	0
				QL12865THB02	45	0
				QL12865THB03	45	0
Unbiased HAST (UHST) [2]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	AD5941	Q14989.UH1	77	0
				Q14989.UH2	77	0
				Q14989.UH3	77	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 168 hrs @ 85°C, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

[2] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Table 3: 0.18µm SiGe BiCMOS at TSMC Fab-4 Fab Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR)	MIL-STD-883, M1015	125°C, 48 Hours	ADA4945-1	Q16405.EL1A	270	0
				Q16405.EL1B	270	0
				Q16405.EL1C	245	0
				Q16405.EL2A	270	0
				Q16405.EL2B	270	0
				Q16405.EL2C	196	0
				Q17557.1.EL1A	300	0
				Q17557.2.EL1B	300	0
				Q17557.3.EL1C	200	0
High Temperature Operating Life (HTOL)	JESD22-A108	125°C<Tj<135°C, Biased, 1,000 Hours	ADA4945-1	Q12802.HO2	77	0
				Q12802.HO3	77	0
				Q12802.HO4	77	0
				Q17557.1.HO	77	0[3]
				Q17557.2.HO2	77	0
				Q17557.3.HO3	77	0[3]
			ADATE330	Q12239.1	32	0
				Q12239.2	32	0
				Q12239.3	32	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	ADATE324	Q12239.16	32	0
Temperature Humidity Bias (THB) [1]	JESD22-A101	85°C, 85%RH, Biased, 1,000 Hours	ADAQ4003	Q13428.1	32	0
				Q13428.2	32	0
				Q13428.3	32	0
			ADATE330	Q12239.6	32	0
Temperature Humidity Bias (THB) [2]	JESD22-A101	85°C, 85%RH, Biased, 1,000 Hours	ADAQ23875	Q16377.TH1	32	0
				Q16377.TH2	32	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

[2] These samples were subjected to preconditioning (per J-STD-020 Level 4) prior to the start of the stress test. Level 4 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 96 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

[3] Six units from the Q17557.1.HO lot had Differential Offset shift (marginal failure) at post-Precon and two units from the Q17557.3.HO3 lot also had the Differential Offset shift at post-500 hours of HTOL. These are guardbanding issue and had been resolved by adjustment of the datasheet limit. This failure is considered an invalid failure and not related to the die revision.

ESD Test Results

The results of Field-Induced Charged Device Model (FICDM) ESD testing is summarized in Table 4. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link on Analog Devices' web site).

Table 4: ADA4945-1 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	16-LFCSP	JS-002	1Ω, Cpkg	±1250V	N/A	C3
HBM	16-LFCSP	ESDA/JEDEC JS-001-2011	1.5kΩ, 100pF	±4000V	N/A	3A

Latch-Up Test Results

Six samples of AD4945-1 were latch-up tested at T_A = +25C per JEDEC Standard JESD78. Class II. Pre- and post-stress electrical test was performed at room and hot temperatures. All pins passed.

Passing Positive Current	Passing Negative Current	Passing Over-Voltage
100 mA	100 mA	8.25 V

Approvals

Reliability Engineer: Ryan Quintin

Additional Information

Data sheets and other additional information are available on Analog Devices' web site